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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/580,755 | 05/30/2000 | Hong Wang | 884.225US1 | 1888 |

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

| EXAMINER |
|---|
| HARKNESS, CHARLES A |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 3 |

DATE MAILED: 09/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

| Office Action Summary | Application No | Applicant(s) | |
|---|---|---|---|
| | 09/580,755 | WANG ET AL. | |
| | Examiner | Art Unit | |
| | Charles A Harkness | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 May 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Papers Submitted*

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Information Disclosure as received on 11/21/00.

### *Election/Restrictions*

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-24, drawn to a two pipeline system with essential code and non-essential code, classified in class 712, subclass 1.

II. Claims 25-30, drawn to compiling or linking of code which consists of non-essential code, classified in class 717, subclass 151.

3. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as being able to execute code that does not have non-essential code present, which would be produced from invention II. See MPEP § 806.05(d).

4. During a telephone conversation with Ann McCrackin on August 27, 2003 a provisional election was made without traverse to prosecute the invention of Wang et al, claims 1-24. Affirmation of this election must be made by applicant in replying to this Office action. Claims 25-30 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the

currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

***Specification***

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

7. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

8. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Watts et al, U.S. Patent Number 5,881,135 (herein referred to as Watts).

9. Referring to claim 1 Watts has taught a processor comprising a first pipeline configured to execute essential code (Watts column 31 lines 21-50);

a second pipeline configured to execute non-essential code (Watts column 31 lines 25-36, column 33 lines 9-12; since the co-processor does not have to be present, the code that is executed by the co-processor is non-essential, even though ); and

a conjugate mapping table configured to specify non-essential code to be executed by the second pipeline (Watts column 23 lines 51-57; it is inherent that some table or list must exist so that the main processor or some other logic device knows to send the floating point operations to the co-processor, and that it would keep all other types of operations for execution in the host, or primary, processor; such a table would be similar to that described in the reference cited, especially since the floating point operations would probably consist of many speech operations in the given environment).

10. Referring to claim 2 Watts has taught wherein the first pipeline is coupled to a first instruction cache configured to cache instructions that determine the logical correctness of a program (Watts column 31 lines 45-50; any normal instructions, including those that would be stored in the cache described would be logical instructions, and thus carrying those instructions out will produce the correct logical results).

11. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Schroter et al, U.S. Patent Number 6,401,192 (herein referred to as Schroter).

12. Referring to claim 1 Schroter has taught a processor comprising a first pipeline configured to execute essential code;

a second pipeline configured to execute non-essential code (Schroter figure 2 figure 3 reference numbers 302 and 304, column 2 lines 43-56, column 3 lines 54-65; the prefetch engine in the prefetch unit only executes hint code, which isn't required for the logical correctness of the program; both the non-prefetch cache unit and the 206 and 210, fixed-point execution unit and floating point unit respectively, from figure 2, are required to execute for the logical correctness of the program and can be seen by the ISA); and

a conjugate mapping table configured to specify non-essential code to be executed by the second pipeline (Schroter abstract, figure 2; in Schroter, it states "in response to a software instruction in an instruction stream, a plurality of prefetch specification data values are loaded into a register having a plurality of entries corresponding thereto" showing that the prefetch hint instruction are in the program code and would require some unit to decide whether to send the instruction on to the 206, 208, or 210 execution units, or have the software hint prefetch unit, 203, execute the instruction).

13. Referring to claim 2 Schroter has taught wherein the first pipeline is coupled to a first instruction cache configured to cache instructions that determine the logical correctness of a program (Schroter figure 2 reference numbers 202, 203, 214; the cache will cache all instructions in the program, including the instructions that determine the logical correctness of the program).

14. Referring to claim 3 Schroter has taught wherein the second pipeline is coupled to a second instruction cache configured to cache instructions that provide hints for the execution of the instructions that determine the logical correctness of the program (Schroter figure 2 reference

numbers 202, 203, 214; the cache will cache all instructions in the program, including the hint instructions).

15. Referring to claim 4 Schroter has taught wherein the first pipeline is coupled to registers that store a micro architectural state, and wherein the conjugate mapping table is responsive to the microarchitectural state (Schroter column 2 lines 43-67; points to prefetch registers which decide which instructions for the first pipeline will be fetched).

16. Referring to claim 5 Schroter has taught further comprising:

a first instruction cache coupled to the first pipeline (Schroter figures 3A, 3B, the caches 214, 326 are coupled to the first pipeline through the lowest level cache); and

a second instruction cache coupled between the conjugate mapping table and the second pipeline (Schroter figure 2 reference numbers 202, 203, 214; the cache will cache all instructions in the program, including the hint instructions).

17. Referring to claim 6 Schroter has taught wherein the conjugate mapping table is responsive to a trigger, the trigger being mapped within the conjugate mapping table to the non-essential code (Schroter abstract, figure 2; in Schroter, it states "in response to a software instruction in an instruction stream, a plurality of prefetch specification data values are loaded into a register having a plurality of entries corresponding thereto" showing that the prefetch hint instruction are in the program code and would require some unit to decide whether to send the instruction on to the 206, 208, or 210 execution units, or have the software hint prefetch unit, 203, execute the instruction).

18. Referring to claim 7 Schroter has taught wherein the conjugate mapping table comprises a plurality of records, each of the plurality of records being configured to map a trigger to a non-

essential code sequence (referring to the rejection of claim 6, the prefetch engine would have to keep a list, or table, or some kind of record of the types of instructions that are hint instructions, so that is knows which instructions to execute and which instructions to pass on to the other execution units).

19. Referring to claim 8 Schroter has taught wherein the trigger comprises an atomic value, such that the conjugate mapping table is configured to specify the non-essential code sequence when the atomic value is satisfied (referring to the rejection of claim 6, the attributes of the instruction would show the prefetch engine if the instruction where a prefetch hint instruction, then the prefetch engine would execute that instruction).

20. Referring to claim 9 Schroter has taught wherein the trigger comprises a vector value, such that the conjugate mapping table is configured to specify the non-essential code sequence when the vector value is satisfied (referring to the rejection of claim 6, the prefetch engine would have to keep a list, or table, or some kind of record of the types of instructions that are hint instructions, so that is knows which instructions to execute and which instructions to pass on to the other execution units).

21. Referring to claim 10 Schroter has taught further comprising a microarchitectural structure coupled between the first pipeline and the second pipeline (Schroter column 2 lines 43-67; points to prefetch registers which decide which instructions for the first pipeline will be fetched).

22. Referring to claim 11 Schroter has taught wherein the microarchitectural structure comprises a register bank (Schroter column 2 lines 43-67; points to prefetch registers).

23. Referring to claim 12 Schroter has taught a processor comprising: an instruction set architecture (ISA) visible path; and a conjugate pipeline coupled to the ISA visible path, the conjugate pipeline being configured to execute hint calculus code and to provide execution hints to the ISA visible path (Schroter figure 2, figure 3 reference numbers 302 and 304, column 2 lines 43-56, column 3 lines 54-65; the prefetch engine in the prefetch unit only executes hint code, which isn't required for the logical correctness of the program; both the non-prefetch cache unit and the 206 and 210, fixed-point execution unit and floating point unit respectively, from figure 2, are required to execute for the logical correctness of the program and can be seen by the ISA).

24. Referring to claim 13 Schroter has taught wherein the processor can take on architectural states and microarchitectural states, the conjugate pipeline being configured to affect microarchitectural states (Schroter column 2 lines 43-67; points to prefetch registers).

25. Referring to claim 14 Schroter has taught wherein the ISA visible path includes a pipeline configured to execute instructions from a user program (Schroter figure 2, figure 3 reference numbers 302 and 304, column 2 lines 43-67, column 3 lines 42-65; it shows that the ISA path executes user programs).

26. Referring to claim 15 Schroter has taught wherein the conjugate pipeline is configured to execute hint calculus code that virtualizes instructions from the user program (Schroter figure 2, figure 3 reference numbers 302 and 304, column 2 lines 43-56, column 3 lines 54-65; Schroter column 2 lines 43-67; points to prefetch registers).

27. Referring to claim 16 Schroter has taught a processor comprising:

a conjugate mapping table coupled to a first pipeline (Schroter abstract, figure 2; in Schroter, it states "in response to a software instruction in an instruction stream, a plurality of prefetch specification data values are loaded into a register having a plurality of entries corresponding thereto" showing that the prefetch hint instruction are in the program code and would require some unit to decide whether to send the instruction on to the 206, 208, or 210 execution units, or have the software hint prefetch unit, 203, execute the instruction), the conjugate mapping table including entries to map triggers from the first pipeline to hint calculus code sequences; and

a second pipeline to execute the hint calculus code sequences (Schroter figure 2 figure 3 reference numbers 302 and 304, column 2 lines 43-56, column 3 lines 54-65; the prefetch engine in the prefetch unit only executes hint code, which isn't required for the logical correctness of the program; both the non-prefetch cache unit and the 206 and 210, fixed-point execution unit and floating point unit respectively, from figure 2, are required to execute for the logical correctness of the program and can be seen by the ISA).

28. Referring to claim 17 Schroter has taught further comprising microarchitectural structures responsive to the second pipeline, the microarchitectural structures being configured to modify states of the first pipeline (Schroter column 2 lines 43-67; points to prefetch registers which decide which instructions for the first pipeline will be fetched).

29. Referring to claim 18 Schroter has taught wherein the microarchitectural structures comprise a branch target buffer (Schroter figure 2 column 2 lines 43-67; the 203 unit is tied directly to the branch unit, 204, which decides which instructions will be sent to the other execution units, with control information and instruction path).

30. Referring to claim 19 Schroter has taught wherein the triggers comprise:

instruction attributes; data attributes; state attributes; and event attributes (referring to the rejection of claim 16, the attributes of the instruction would show the prefetch engine if the instruction where a prefetch hint instruction, then the prefetch engine would execute that instruction).

31. Referring to claim 20 Schroter has taught further comprising:

an instruction cache coupled between the conjugate mapping table and the second pipeline, the instruction cache being configured to cache the hint calculus code sequences (Schroter figure 2 reference numbers 202, 203, 214; the cache will cache all instructions in the program, including the hint instructions).

32. Referring to claim 21 Schroter has taught wherein the processor is configured to execute essential code and non-essential code, and wherein the non-essential code comprises the hint calculus code sequences (Schroter abstract figure 2 figure 3 reference numbers 302 and 304, column 2 lines 43-56, column 3 lines 54-65).

33. Referring to claim 23 Schroter has taught wherein the second pipeline is configured to implement built-in-self-test (Schroter column 8 lines 17-33; the prefetch is shown to do a test; since the claim is broad, any testing can reject such a claim, that is done by the second pipeline).

34. Referring to claim 24 Schroter has taught wherein the second pipeline is configured to implement instruction set virtualization (Schroter figure 2, figure 3 reference numbers 302 and 304, column 2 lines 43-56, column 3 lines 54-65; Schroter column 2 lines 43-67; points to prefetch registers).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schroter.

36. Referring to claim 22 Schroter has not taught wherein the second pipeline is configured to implement register file expansion for forward compatibility across different generations of processors. Official Notice is taken, that it would be an obvious improvement to make an invention so that other generations of processors will be able to use the same invention. One of ordinary skill in the art at the time of the invention would have recognized the benefit in preparing the system for forward compatibility with other processors. The improvement of expanding the register file would be obvious, since the register files have increase with different processors.

***Conclusion***

37. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Mills et al, U.S. Patent Number 6,205,544 has taught decomposition of instructions into branch and sequential code sections, using different execution units.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

August 29, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100